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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/615,846

07/10/2003

Hirohisa Nakayama

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08/05/2004

OLIFF & BERRIDGE, PLC

P.O. BOX 19928

ALEXANDRIA, VA 22320

EXAMINER

SMOOT, STEPHEN W

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/615,846	<b>Applicant(s)</b> NAKAYAMA, HIROHISA	
	<b>Examiner</b> Stephen W. Smoot	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

This Office action is in response to application papers filed on 10 July 2003.

### ***Specification***

1. The disclosure is objected to because of the following informality:

On page 16, line 4, change "adhesive layer 82" to --adhesive layer 84-- because the adhesive layer is designated as reference number 84 in Fig. 6 and elsewhere in the written description (see page 15, line 19 to page 16, line 12).

Appropriate correction is required.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Semiconductor Package with a Chip Mounted on a Sheet that Includes at Least One Lead Bonded to the Sheet and Another Lead Not Bonded to the Sheet.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3-4, 9, 11-12, 18-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the first leads" in line 2. There is insufficient antecedent basis for this limitation in the claim. That is, claim 1 (from which claim 3 depends) does not provide antecedence for plural first leads (see claim 1, line 7).

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, because it depends on claim 3.

Claim 9 recites the limitations "the position under the center" in lines 2-3 and "the width" in line 4. There is insufficient antecedent basis for these limitations in claim 9.

Claim 11 recites the limitation "the first leads" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitations "the first leads" in line 3 and "the midpoints of the sides" in line 3. There is insufficient antecedent basis for these limitations in claim 12.

Claim 18 recites the limitation "the first leads" in line 2. There is insufficient antecedent basis for this limitation in the claim. That is, claim 16 (from which claim 18 depends) does not provide antecedence for plural first leads (see claim 16, line 7).

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, because it depends on claim 18.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-7, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Okinaga et al. (US 5,234,866).

Referring to Figs. 1, 2 and column 2, line 40 to column 3, line 23, Okinaga et al. disclose a package structure with the following features:

- A semiconductor pellet (i.e. chip) (1) attached to an insulating sheet (5) with an adhesive layer (6);
- The insulating sheet (5) is bonded to some of the leads (2), but there are some leads that are not bonded to the insulating sheet (5) as shown in Fig. 2;

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- Bond pads (7) on the pellet (1) are electrically connected to the leads (2) using bond wires (8) (also see column 4, lines 3-14);
- The insulating sheet (5) and bond wires (8) are bonded to the same surface of the leads as shown in Figs. 1, 2; and
- The structure is sealed in resin (4) to form a package (3) with outer lead portions extending outside the resin (4) as shown in Figs. 1, 2.

These are all of the limitations set forth in claims 1, 3, 5-7 of the applicant's invention. Regarding the method claims 16, 18, the above package is assembled by bonding the insulating sheet (5) to a lead frame, using an adhesive (6) to attach the pellet (1) to the insulating sheet (5), wire bonding the bond pads (7) to tip portions (2b) of the leads (2), and sealing the assembly in resin (4) (see column 2, lines 45-53 and column 4, lines 15-27). Regarding structure claim 2 and method claim 17, Figs. 6, 7 correspond to an alternative example, in which the insulating sheet (5) and bond wires (8) are bonded to opposite surfaces of the leads (also see column 5, line 24 to column 6, line 9).

7. Claims 1-2, 7, 12, 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Corisis (US 6,218,216 B1).

Referring to Figs. 3, 4 and column 4, line 52 to column 6, line 11, Corisis ('216) discloses a package structure with the following features:

- A lead frame (76) includes a set (104) of inner leads (78) that are adhesively joined to a semiconductor die (72) with an intervening insulative layer (92);

- Some of the leads (78) corresponding to lead set (104) are disposed near midpoints corresponding to sides of the die (72) as shown in Fig. 3;
- The lead frame (76) includes sets (100, 102) of inner leads (78) that are not bonded to the intervening insulative layer (92);
- The inner leads (78) are electrically connected to bond pads (84) formed on the semiconductor die (72) using bond wires (98);
- The insulative layer (92) and bond wires (98) are bonded to opposite surfaces of the leads (78) as shown in Figs. 3, 4;
- The structure is encapsulated to form a device package; and
- The external leads of the device package are typically mounted on a circuit board in order to electrically interconnect the packaged die to an external electrical host apparatus (also see column 1, lines 25-29).

These are all of the limitations set forth in claims 1-2, 7, 12, 14-15 of the applicant's invention. Regarding the method claims 16-17, the above package is assembled by using an insulative layer (92) to adhesively join a semiconductor die (72) to a lead frame (76), wire bonding the bond pads (84) to inner leads (78), and encapsulating the assembly to form a package.

8. Claims 1-2, 5-8, 10, 12, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kinsman (US 6,265,764 B1).

Referring to Figs. 8, 9 and column 6, line 13 to column 7, line 10, Kinsman discloses a package structure with the following features:

- A lead frame (14) includes two buses (58A, 58B) with sequentially alternating legs (36A, 36B) that are joined to a semiconductor die (30) with insulative members (66);
- The insulative members (66) may be strips of polymer such as adhesive coated polyimide tape and, as shown in Figs. 8, 9, two strips extend to the left and right of the die's (30) center resulting in an open center portion with respect to the presence of polyimide tape;
- The lead frame includes inner leads (22A) that are not bonded to the insulative members (66);
- The inner leads (22A) and the sequentially alternating legs (36A, 36B) are electrically connected to bond pads (46) of the semiconductor die (30) using bond wires (60, 60A, 60B);
- The insulative members (66) and bond wires (60A, 60B) are bonded to the opposite surfaces of the buses (58A, 58B) as shown in Figs. 8, 9; and
- The structure is encapsulated to form a package (also see column 4, lines 24-27).

These are all of the limitations set forth in claims 1-2, 5-8, 10, 12 of the applicant's invention. Regarding the method claims 16-17, the above package is assembled by providing a lead frame and using die attach, wire bonding, and encapsulating steps to form the package (see column 4, lines 24-27).

9. Claims 1, 3, 5-7, 12-13, 16, 18, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Corisis (US 6,277,673 B1).

Referring to Fig. 4 and column 6, line 55 to column 8, line 3, Corisis ('673) discloses a package structure with the following features:

- A lead frame (10") including lead fingers (18") with portions (24") for supporting a semiconductor device (100");
- The lead frame portions (24") are adhesively attached to the semiconductor device (100") using a tape (40") and a silver filled epoxy paste adhesive material;
- Some of the lead frame portions corresponding to die paddle portions (30") are disposed near midpoints corresponding to sides of the device (100") as shown in Fig. 4;
- The lead frame (10") includes lead fingers (12") with inner leads (13") that are not bonded to the tape (40");
- The lead fingers (12", 18") are electrically connected to bond pads (102") formed on the semiconductor die (100") using bond wires (50");
- At least one of the lead fingers (18") as shown in Fig. 4 is not electrically connected with bond wires (50") (e.g. the top lead finger shown on the left side of Fig. 4);
- The tape (40") and bond wires (50") are bonded to the same surface of the lead fingers (12", 18") as shown in Fig. 4; and
- The structure is encapsulated in epoxy plastic to form a package (200").

These are all of the limitations set forth in claims 1, 3, 5-7, 12-13 of the applicant's invention. Regarding the method claims 16, 18, 20, the above package is assembled by using a tape (40") to adhesively join a semiconductor device (100") to a lead frame (10"), wire bonding the bond pads (102") to lead fingers (12", 18"), and encapsulating the assembly to form the package.

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kohara, Huang et al., Ikenaga et al., and Kunimatsu et al. teach lead frames that feature at least one lead bonded to a sheet that supports a semiconductor chip and another lead that is not bonded to the sheet.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

*Stephen W. Smoot*  
Patent Examiner  
Art Unit 2813